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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/052,989	11/09/2001	Han-Kun Hsieh	YUSO-131	1309

7590
Raymond Sun
12420 Woodhall Way
Tustin, CA 92782

08/18/2005

EXAMINER

VU, DAVID

ART UNIT	PAPER NUMBER
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2818

DATE MAILED: 08/18/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/052,989

Applicant(s)

HSIEH ET AL.

Examiner

DAVID VU

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 27 May 2005.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 24-33,44 and 45 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 24-33,44 and 45 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 09 November 2001 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved by the Examiner.
- If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

- 13) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
- a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

- 1) ☐ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____
- 4) ☐ Interview Summary (PTO-413) Paper No(s). _____
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other:

DETAILED ACTION

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

1. Claims 24-27; 32-33 and 44 are rejected under 35 U.S.C. 103 (a) as being unpatentable over Higdon et al. (US Pat. 6,375,062) in view of Koshio (US Pat. 6,392,143).

Regarding claims 24 and 44, Higdon discloses a method of forming electroplated solder for making flip chip joints and board to board solder joints, comprising: providing a flexible circuit 11 (col. 1, lines 23-25) including a surface bearing electrical circuitry that includes at least a contact pad 16 (col. 4, lines 34-38); forming a solder mask layer 12 on surface, solder mask 12

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being patterned to expose contact pad 16 (col. 4, lines 25-34); forming a thin metal seed layer 20 over surface, seed layer 20 being solely made of a first metal material (col. 5, lines 9-12); forming a resist layer 22 with at least one opening located at contact pad 16 that is deposited over seed layer 20 (col. 5, lines 17-26 and fig. 1); forming a solder bump 26 in opening by electroplating, solder bump containing at least first metal material (col. 5, lines 26-30 and 42-44 and fig. 1); and removing resist layer 22 and seed layer 20 beneath resist layer 22 (col. 6, lines 54-56 and fig. 3); wherein seed layer 20 beneath solder bump 28 dissolves completely into solder bump 28 after a reflow process, and disappears (col. 5, lines 44-49 and fig. 4).

Higdon discloses the substrate/circuit board may be a flexible circuit (col. 1, lines 23-25) but fails to disclose the substrate is an organic circuit board. However, Koshio teaches the flexible substrate is formed of an organic substrate (col. 6, lines 14-18). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the invention of Higdon by forming an organic substrate as taught by Koshio since the material such as an organic circuit board is recognized equivalent material for forming a flexible circuit in a method of manufacturing a semiconductor device.

Regarding claim 25, Higdon discloses first metal material 20 is copper (col. 5, lines 12-15).

Regarding claim 26, Higdon discloses seed layer 20 is 0.15-0.25 micrometer thick (less than 0.005 millimeter).

Regarding claim 27, Higdon discloses seed layer 20 is made of physical vapor deposition by sputtering method (col. 5, lines 9-12).

Regarding claim 32, Higdon discloses before forming thin metal seed layer 20, forming a barrier layer 18 on contact pad 16 (col. 4, lines 39-65).

Regarding claim 33, Higdon discloses barrier layer 18 is made of copper, nickel; chromium, titanium, copper-chromium alloy (col. 4, lines 39-65).

2. Claims 28 and 29 are rejected under 35 U.S.C. 103 (a) as being unpatentable over Higdon et al. (US Pat. 6,375,062) and Koshio (US Pat. 6,392,143) as applied to claims 24 above, and further in view of Inaba et al. (US Pat. 6,387,734, herein after Ibana).

The combination of Higdon and Koshio discloses a method of forming electroplated solder as describe above. However, Higdon and Koshio fail to disclose seed layer is made of chemical vapor deposition or electroless plating method. Inaba teaches seed layer is formed by chemical vapor deposition or electroless plating method (col. 5, lines 40-49). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the invention of Higdon and Koshio by depositing a seed layer as taught by Inaba, in order to provide the well-known advantageous benefit of a smooth surface.

3. Claims 30 and 31 are rejected under 35 U.S.C. 103(a) as being unpatentable over Higdon et al. (US Pat. 6,375,062); Koshio (US Pat. 6,392,143) and Inaba et al. (US Pat. 6,387,734) as applied to claims 24 and 29 above, and further in view of Donovan et al. (US Pat. 3,958,048, herein after Donovan).

The combination of Higdon, Koshio and Inaba discloses a method of forming electroplated solder as describe above. However, Higdon, Koshio and Inaba fail to disclose

performing a reduction process of copper ions to form a thin copper film on surfaces, wherein there is no reduction of noble metal ions such as palladium or platinum. Donovan teaches a process for electroless plating a copper layer by coating the surfaces with aqueous solutions which at least contains copper ions and then performing a reduction process of copper ions to form a thin copper film on surfaces, wherein there is no reduction of noble metal ions such as palladium or platinum (col. 8, lines 50-59). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the invention of Higdon, Koshio and Inaba by depositing a seed layer as taught by Donovan, because the manufacture of the model chip scale package would have been relatively simplified and economical (col. 3, lines 54-60).

4. Claim 45 is rejected under 35 U.S.C. 103 (a) as being unpatentable over Higdon et al. (US Pat. 6,375,062) and Koshio (US Pat. 6,392,143) as applied to claims 24 above, and further in view of Bhatt et al. (US Pat. 5,822,856, herein after Bhatt).

The combination of Higdon and Koshio disclose a method of forming electroplated solder on an organic circuit board as describe above but fails to disclose the material of organic circuit board. Bhatt teaches organic circuit board is formed of epoxy, polyimide (col. 3, lines 57-63). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the invention of Higdon and Koshio by using the material of organic circuit board as taught by Bhatt since the material such as epoxy, polyimide is recognized equivalent material for forming the organic circuit board in a method of manufacturing a semiconductor device.

Conclusion

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to David Vu whose telephone number is (571) 272-1798. The examiner can normally be reached on Monday-Friday from 8:00am to 5:00pm. If attempt to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Nelms can be reached on (571) 272-1787. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR, Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



David Vu

August 16, 2005